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Ho et al.

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(54) **BOTTOM SOURCE SUBSTRATELESS POWER MOSFET**

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H01L 29/78 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 29/7827*** (2013.01)

(58) **Field of Classification Search**
CPC H01L 29/78; H01L 21/283
USPC 257/330, E29.262, E21.19, E21.159, 257/692, 676, 737, 738; 438/586
See application file for complete search history.

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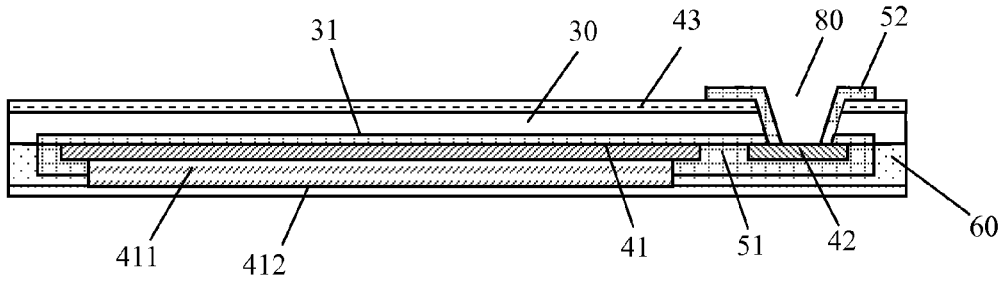
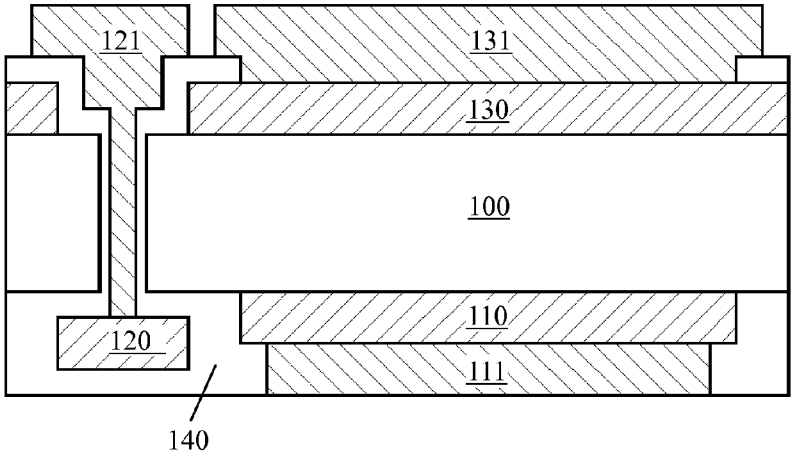
(57) **ABSTRACT**

A bottom source power metal-oxide-semiconductor field-effect transistor (MOSFET) device includes a gate electrode and a source electrode formed on an initial insulation layer on a first surface of a semiconductor chip and a drain electrode formed on a second surface of the semiconductor chip. The source electrode includes a source metal, a source electrode bump formed on the source metal and a source electrode metal layer on top of the source electrode bump. A first insulation layer covers the gate electrode. A through via aligned to the gate electrode is formed from the second surface of the chip to expose a portion of the gate electrode from the second surface.

9 Claims, 6 Drawing Sheets




121
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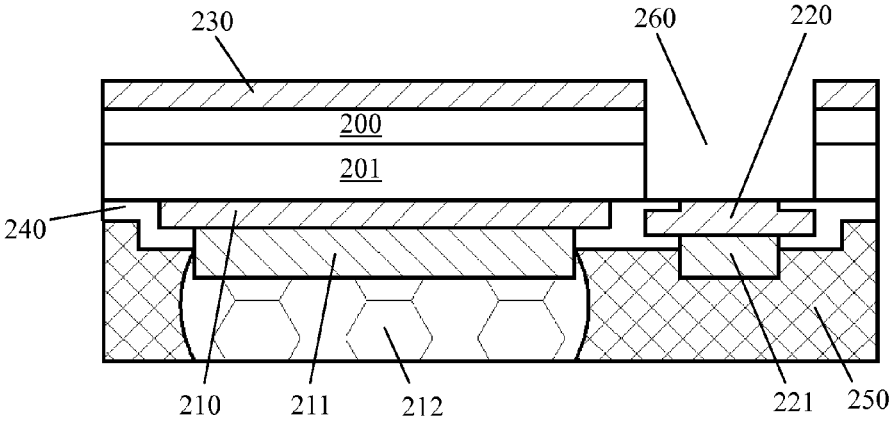
111
140

FIG. 1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221
250

FIG. 2

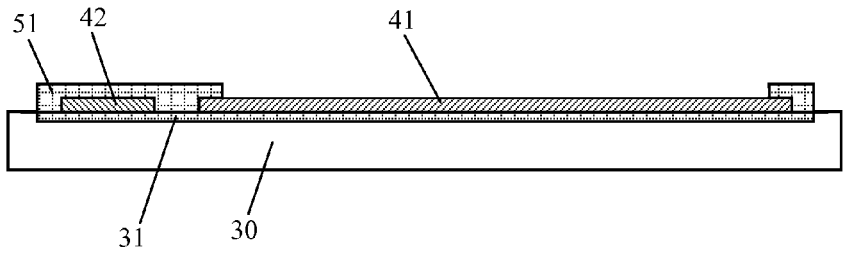


FIG. 3

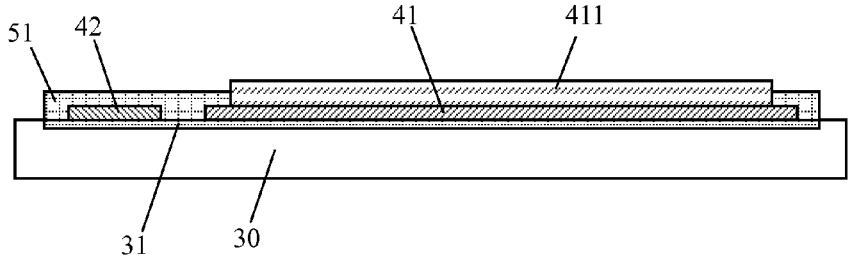


FIG. 4

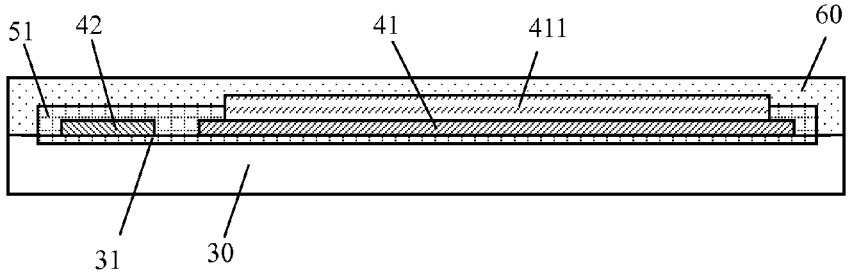


FIG. 5

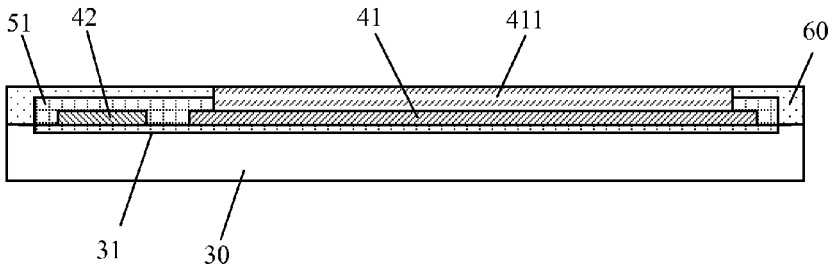


FIG. 6

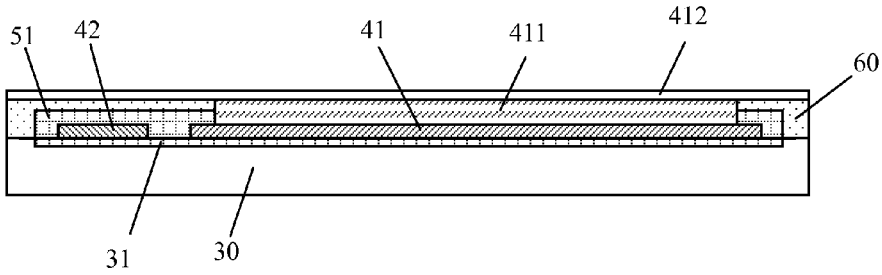


FIG. 7

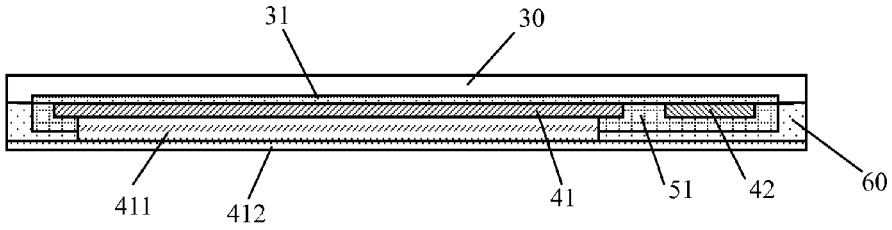


FIG. 8

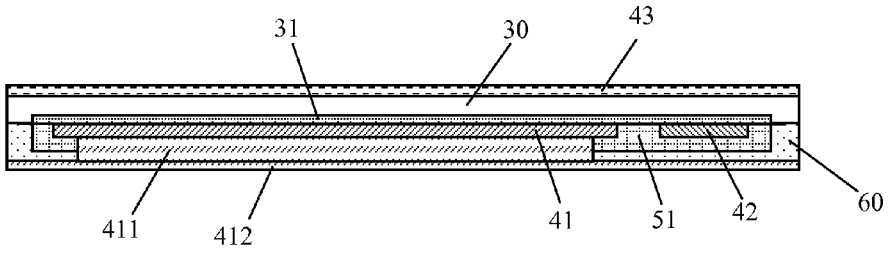


FIG. 9

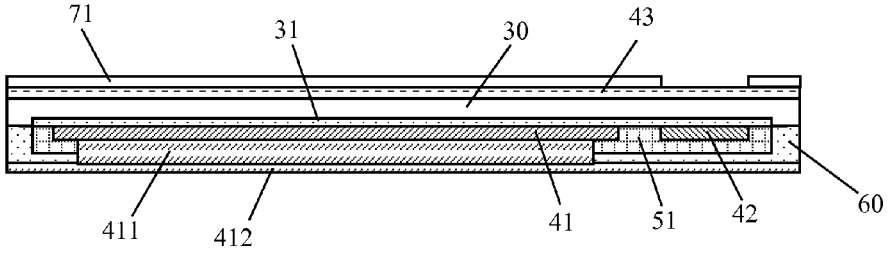


FIG. 10

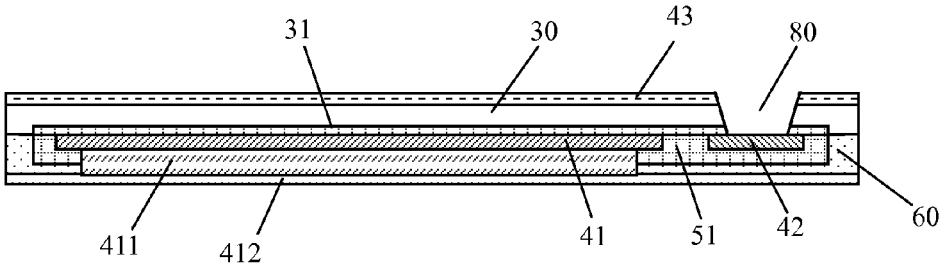


FIG. 11

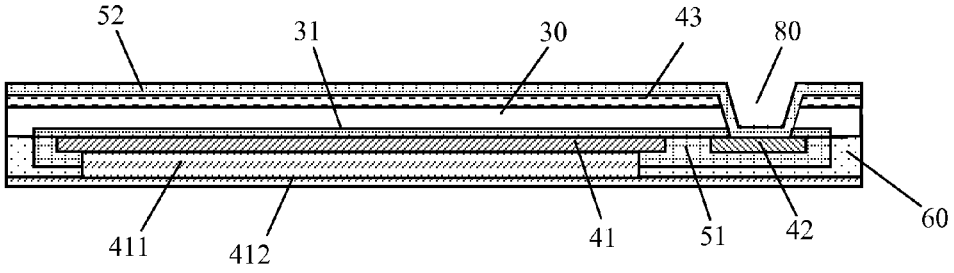


FIG. 12

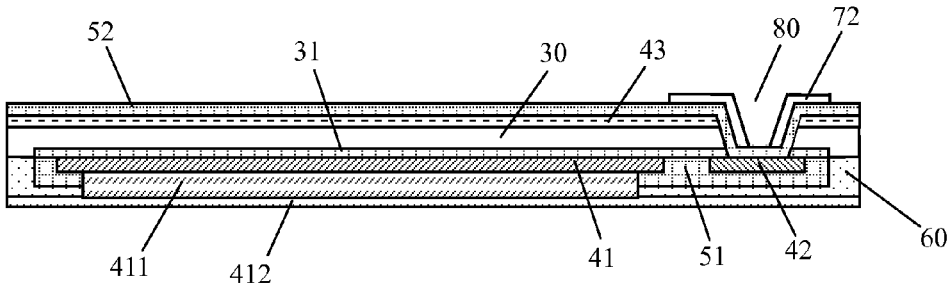
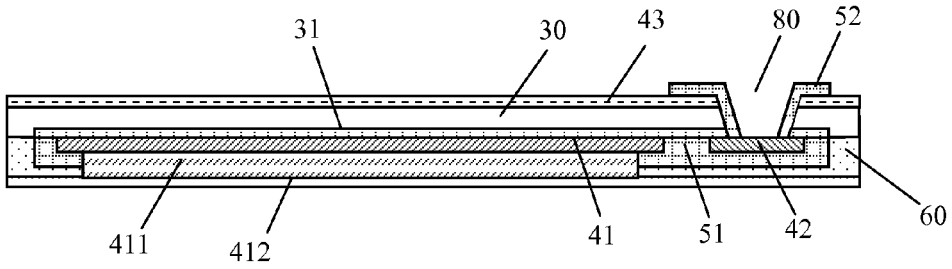

52
31
30
43
80
72
411
412
41
51
42
60

FIG. 13


31
30
43
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411
412
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51
42
60

FIG. 14

BOTTOM SOURCE SUBSTRATELESS POWER MOSFET

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a divisional application of a pending U.S. patent application entitled "BOTTOM SOURCE POWER MOSFET WITH SUBSTRATELESS AND MANUFACTURING METHOD THEREOF" by Yueh-Se Ho et al with application Ser. No. 13/273,219, and filing date of Oct. 13, 2011 whose content is hereby incorporated by reference for all purposes.

FIELD OF THE INVENTION

The invention relates to a semiconductor device and manufacturing method thereof, in particular to a substrateless bottom source power MOSFET device and a manufacturing method thereof.

BACKGROUND OF THE INVENTION

A vertical power MOSFET device usually has a source electrode formed of a source metal layer and a gate electrode formed of a gate metal layer disposed on a top surface of the semiconductor chip and a drain electrode formed of a drain metal layer on a bottom surface of the semiconductor chip. A bottom source power MOSFET chip having a source electrode on one surface and the gate electrode and the drain electrode on the other surface is preferred in applications such as stacked die co-package structure used in a DC-DC converter. In other applications, bottom source power MOSFET chip is required, for example, when the die paddle of a lead frame package is used as the ground electrode.

SUMMARY OF THE INVENTION

The present invention provides a bottom source power MOSFET device comprising a drain electrode, a gate electrode and a source electrode electrically insulated from each other for electrically connecting to the external device. The source electrode is formed at a first surface of a semiconductor chip that is flipped with the first surface facing downward, thus the source electrode is exposed at the bottom of the power MOSFET device. As such, the drain electrode formed at a second surface of the chip is exposed at the top of the power MOSFET device. A gate electrode formed at the first surface of the chip is partially exposed from a through via formed on the second surface of the chip, thereby providing access to the gate electrode from the top of the power MOSFET device.

The semiconductor chip comprises a substrate and an initial insulation layer formed on a first surface of the substrate. When the first surface of the chip is upward, a source metal is formed on the initial insulation layer of the chip, a source electrode bump is formed on the source metal and a source electrode metal layer is formed on the source electrode bump. The source metal and a gate metal are respectively formed on the initial insulation layer and are electrically insulated from each other. A first insulation layer is deposited on the gate metal and the source metal with a portion of the top surface of the source metal exposed from the first insulation layer. The source electrode bump is made of a metal on the exposed portion of source metal by electroplating.

A molding compound is deposited covering the first insulation layer and the external surface of the source electrode bump. The molding compound is then ground to expose the top surface of the source electrode bump. A source electrode metal layer is formed on the top surface of the source electrode bump and the molding compound ready for electrically connecting to the external devices.

The chip is ground at its second surface to reduce its thickness to a substrateless level. A drain metal layer is formed to cover the second surface of the chip substrate via metallization forming a drain electrode for electrically connecting to the external devices. A through via aligned to the gate metal penetrates through the drain metal layer, the substrate and the initial insulation layer reaching the gate metal. The through via can be formed via a laser drilling method. Alternatively, the through via can be formed by wet or dry etching method. In this etching method, a first mask is firstly applied on the top surface of the drain electrode metal layer, which includes an opening corresponding to the position of the gate electrode. A wet or a dry etching is carried out through the opening in the first mask, etching down through the drain electrode metal layer, substrate and initial insulation layer to form the though via with portion of the second surface of the gate electrode exposed from the through via.

A second insulation layer is formed at the second surface of the chip to cover the top surface of the drain electrode metal layer and the side wall and bottom of the through via. A second mask is applied on the second insulation layer, covering the sides of the through via and portions of the second insulation layer surrounding the through via. The second insulation layer not covered by the second mask is removed by etching. As such, the side wall of the though via and portions of the drain electrode metal layer surrounding the through via in a certain distance are covered by the second insulation layer, while the bottom of the through via is not covered by the second insulation layer with a portion of the gate metal exposed from the bottom of the through via forming a gate electrode.

The present invention provides a bottom source power MOSFET device and a manufacturing method thereof, with the source electrode exposed at the bottom of the device, and the drain electrode and the gate electrode exposed at the top of the device and electrical isolated from each other. The method of the present invention is simple and effectively reduces the number of mask used (only two masks) during the process and can be applied for a thin chip, i.e., with a thickness of substrateless level. An insulation protection is carried out between the drain electrode and the gate electrode area via the second insulation layer in the through via and the initial insulation layer of the backside of the gate electrode, therefore short circuit between the drain electrode and the gate electrode can be effectively prevented.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross-sectional schematic diagram of a bottom source power MOSFET device according to present invention.

FIG. **2** is a cross-sectional schematic diagram of another bottom source power MOSFET device according to present invention.

FIGS. **3** to **14** are cross-sectional schematic diagrams illustrating a process flow for manufacturing of power MOSFET device of the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

FIG. **1** is a cross-sectional diagram illustrating a power MOSFET device according to this invention. The power

MOSFET chip **100** includes a gate metal layer **120** and a source metal layer **110** formed correspondingly at a first surfaces of the chip **100**, and a drain metal layer **130** formed correspondingly on the second surface of the chip. A solderable source electrode metal layer **111** is deposited on the source metal layer **110** and a solderable drain electrode metal layer **131** is deposited on the drain metal layer **130**. As shown in FIG. **1**, the power MOSFET chip **100** is flipped with its first surface at the bottom and its second surface at the top of the semiconductor device. A through via is formed through the chip **100**, which is lined with a thin dielectric layer and then filled with a metal forming a gate electrode extension **121**, one end of which is electrically connected to the gate electrode metal layer **120** and the other end extending and exposing at the second surface of the power MOSFET chip or the top surface of the semiconductor structure forming a gate electrode for electrically connecting to external devices. The gate electrode extension **121** is also electrically insulated from the substrate of chip **100**, the drain electrode metal **130** and drain soldering layer **131** via a dielectric layer.

Furthermore, a passivation layer **140** is formed for electrically isolating the source metal layer **110** and the solderable source electrode metal layer **111** from the gate metal layer **120** by completely encapsulating the gate metal layer **120** inside the passivation layer **140**. The solderable source electrode metal layer **111** and the solderable drain electrode metal layer **131** are respectively exposed forming the drain electrode and the source electrode for electrically connecting to the external devices. As shown in FIG. **1**, the gate electrode and the drain electrode are located at the top of the power MOSFET device, while the source electrode is located at the bottom of the power MOSFET device.

FIG. **2** is a cross-sectional diagram illustrating another conventional power MOSFET device. As shown in FIG. **2**, the power MOSFET device includes a source electrode at bottom of the device and an initial layer **201** of silicon oxide formed at the first surface of the chip substrate **200**. A gate metal **220** and a source metal **210** are formed at the initial insulation layer **201**, with a gate electrode metal layer **221** and a source electrode metal layer **211** correspondingly formed at the gate metal **220** and the source metal **210**. The gate metal **220** and the gate electrode metal layer **221** are electrically insulated from the source metal **210** and the source electrode metal layer **211** via an electrical insulation layer **240**. A solder ball **212** is placed on the source electrode metal layer **211**. The gate electrode metal layer **221** and the solder ball **212** exposed out of the insulation layer **240** are encapsulated by a molding compound **250**. The bottom surface of the solder ball **212** is exposed out of the bottom surface of the molding compound **250**, thereby forming the source electrode area for electrically connecting to the external devices.

A drain metal layer **230** located at the second surface of the chip substrate **200** corresponding to the top of the power MOSFET device is used as the drain electrode for electrically connecting to the external devices. A through via **260** is formed correspondingly to the position of the gate electrode **220**, which penetrates through the drain metal layer **230**, the chip substrate **200** and the initial insulation layer **201** and stops at the surface of the gate electrode **220**, thereby forming a gate electrode area for electrically connecting to the external device. In this structure, the drain electrode and the exposed gate electrode in the through via **260** are located at the top side of the power MOSFET device, while the source electrode area is located at the bottom side of the power MOSFET device. Preferably the side wall of the through via **260** should be lined with an insulation layer as that shown in FIG. **14**, to prevent a circuit short between the gate electrode and the drain, which generally extends from the bulk of substrate to the side wall of the through via.

FIG. **14** is a cross-sectional schematic diagram of a preferred embodiment of a bottom source power MOSFET device of the present invention and FIGS. **3-14** are the process steps of making the device according to present invention. In this power MOSFET device, the drain electrode and the gate electrode are exposed at the top side of the device for electrically connecting to the external devices, while the source electrode is exposed at the bottom side of the device.

Referring to FIG. **3**, an initial insulation layer **31** is formed on a first surface of the substrate **30** of a semiconductor chip. In one embodiment an edge of the initial insulation layer **31**, such as an oxide, extends to a distance away from the edge of substrate. A gate metal **42** and a source metal **41** are formed on the initial insulation layer **31** with an edge of the gate metal and an edge of the source metal recess from the edges of the initial insulation layer **31**. A first insulation layer **51**, such as an oxide or nitride, is deposited having an edge extending beyond the edge of the gate metal layer to encapsulate the gate metal **42**, to fill the space between the gate metal **42** and the source metal **41**, and to cover the sides and portions of the top surface at the edge of the source metal **41** to prevent short circuit.

Referring to FIG. **4**, a metal source electrode bump **411** is formed on the exposed surface of the source metal **41** that is not covered by the first insulation layer **51** via electroplating. The top surface of the source electrode bump **411** is higher than that of the first insulation layer **51**. The source electrode bump **411** and the gate metal **42** are electrically insulated from each other via the first insulation layer **51**.

Referring to FIG. **5**, a dielectric material **60**, such as a molding compound or silicon oxide, of a predetermined thickness is deposited on top of the structure to encapsulate the first insulation layer **51** and the source electrode bump **411**. The dielectric material may extend to the edge of the substrate. As shown in FIG. **6**, the dielectric material **60** may be ground or polished from its top surface to expose the top surface of the source electrode bump **411**. As shown in FIG. **7**, a source electrode metal layer **412** is deposited on the top surface of the source electrode bump **411** and the molding compound **60**, which is connected with the source electrode **41** via the source electrode bump **411**, thereby forming a source electrode of the semiconductor chip for electrically connecting to the external devices. The source electrode metal layer extends to the edge of the semiconductor substrate.

Referring to FIG. **8**, the chip is flipped, thus the source electrode is located at the bottom side of the power MOSFET device. The second surface of the substrate **30** of the chip is ground to reduce its thickness to substrateless level, for example, 10 microns or thinner. In some applications, the chip is thinned to 4 microns or 2 microns. A drain metal layer **43** is formed to cover the whole second surface of the substrateless chip **30** to form a drain electrode for connecting to the external devices as shown in FIG. **9**.

As shown in FIG. **10**, a first mask **71**, which includes an opening aligned to the gate electrode **42**, is applied on the top surface of the drain electrode metal layer **43**. Wet and/or dry etching is performed through the opening on the first mask from the backside of the thinned chip and into the drain electrode metal layer **43**, the substrate **30** and the initial insulation layer **31** and ends at the gate electrode **42** to form a through via **80** as shown in FIG. **11**. The first mask is then removed. Alternatively, the through via **80** may be formed by laser drilling without the use of mask **71**.

A second insulation layer **52** is deposited to cover the drain metal layer **43** and the bottom and side wall of the through via **80** as shown in FIG. **12**. The second insulation layer **52** extends to the bottom and along the side wall of the through via **80**, thus connecting to the initial insulation layer **31**.

As shown in FIG. **13** and FIG. **14**, a second mask **72** is applied on the second insulation layer **52**, which includes an opening at the gate electrode **42** at the bottom of the through via **80**. The second insulation layer **52** covered by the second mask **72** is retained via etching or similar process, while the exposed area of the second insulation layer **52** is removed. Specifically, the second insulation layer **52** on the side wall of the through via **80** and in the area above the drain electrode metal layer **43** surrounding the through via **80** in a certain distance is retained, while the rest of the second insulation layer **52** at the top surface of the drain electrode metal layer **43** and the bottom of the through via **80** are removed. The exposed part of the drain metal layer **43** and the exposed part of the gate metal **42** form the drain electrode and the gate electrode respectively of the power MOSFET device for connecting to the external devices.

As shown in FIG. **14**, in the power MOSFET device of this invention, the drain electrode and the gate electrode are located at the top side of the device, while the source electrode area is located at the bottom side of the device. Furthermore, the drain electrode and the gate electrode are electrically insulated and protected by the second insulation layer **52** in the through via **80** and the initial insulation layer **31**, therefore short circuit between the drain electrode and the gate electrode can be effectively prevented.

The chip thickness of the present invention power MOSFET device is at substrateless level and the overall manufacturing process for making thinned power MOSFET device only uses two masks. In case laser drilling method is used to form the through via **80**, only one mask (second mask **72**) is used in the manufacturing process.

Although the content of the present invention has been introduced in detail through above preferred embodiments, it should be recognized that above descriptions should not be regarded as the limitation to the invention. Various changes and variations are undoubtedly obvious for the technical personnel of the field after reading the specification. Therefore, the protection scope of the invention shall be limited by the attached claims.

The invention claimed is:

1. A bottom source power MOSFET device comprising:

a semiconductor chip having a drain electrode, agate electrode and a source electrode electrically insulated from each other,

wherein the source electrode being formed at a first surface of the semiconductor chip with the first surface of the semiconductor chip facing downward and the source electrode being exposed at a bottom of the power MOSFET device; the drain electrode being formed at a second surface of the semiconductor chip opposite to the first surface and being exposed at a top of the power MOSFET device; the gate electrode being formed at the first surface of the semiconductor chip with a portion of the gate electrode being exposed through a through via formed from the second surface to the first surface of the semiconductor chip, a side wall of the through via being covered with an insulation layer, wherein the gate electrode being exposed from the top of the power MOSFET device;

wherein the semiconductor chip comprising a substrate and an initial insulation layer formed on a surface of the substrate; the source electrode comprising a source metal layer formed directly on a surface of the initial insulation layer, a source electrode bump formed on the source metal layer and a source electrode metal layer formed on the source electrode bump, the source electrode metal layer having a top surface area larger than a top surface area of the source electrode bump; the gate electrode comprising a gate metal formed on the surface of the initial insulation layer, a first insulation layer covering the entire gate metal and extending over an edge portion of the source metal not covered by the source electrode bump.

2. The bottom source power MOSFET device of claim **1** wherein a surface of the source electrode bump extending beyond the first insulation layer and a molding compound encapsulating the first insulation layer having a surface coplanar to the surface of the source electrode bump.

3. The bottom source power MOSFET device of claim **2**, wherein the source electrode metal layer formed on the source electrode bump extending over the surface of the molding compound to an edge of the molding compound.

4. The bottom source power MOSFET device of claim **1**, wherein the semiconductor chip being ground from its second surface to reduce its thickness to less than 2 microns.

5. The bottom source power MOSFET device of claim **4**, wherein the drain electrode comprising a drain metal layer deposited on the ground second surface.

6. The bottom source power MOSFET device of claim **5**, wherein the through via penetrates through the drain metal layer, the substrate and the initial insulation layer, and wherein the insulation layer covering the side wall of the through via and a portions of drain metal layer surrounding the through via.

7. The bottom source power MOSFET device of claim **1**, wherein the initial insulation layer extending to a distance away from an edge of the semiconductor substrate.

8. The bottom source power MOSFET device of claim **7**, wherein the gate metal layer extending to a distance away from the edge of the initial insulation layer and the first insulation layer extending beyond an edge of the gate metal layer therefore encapsulating the edge of the gate metal layer.

9. The bottom source power MOSFET device of claim **8**, wherein the source electrode metal layer extending to the edge of the semiconductor substrate.

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